C0-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Explain Von-Neumann architecture.
b) Explain Arithmetic micro operation.
c) What are the desirable properties of RISC architecture?
d) Explain SISD and SIMD architecture.
e) What are the difference between scalar instructions and vector instructions? Give at least four differences.
f) Perform 2's complement operation on $(1110011)_2$.
g) Define Program Control.

(7x4)

2.

a) What could be the maximum size of cache memory, depending on the addressing capacity of a processor? Justify your answer. Why cache memory is also known as associative memory as well as content addressable memory?
b) Briefly explain the address mapping techniques of cache memory.
c) Briefly explain 'cache coherence' problem. Identify the major reasons for cache coherence problem.

(6+6+6)

3.

a) You are given two n-bit comparators. Each comparator, given numbers A and B, provides outputs to indicate A> B, A = B, A < B. Indicate how these can be connected in cascade to form a 2n-bit comparator.
b) Compare and contrast 1's complement and 2's complement representation of integer numbers.
c) Write the sequence of steps required to perform division of two double precision numbers using a single precision computer.

(7+4+7)

4.

a) Briefly explain the working principle of pipelined architecture. For a given number of stages of the processor, a number of tasks and period of synchronizing clock, find the speedup and efficiency of the pipelined processor.
b) What is data hazard? Briefly explain with a suitable example.
c) Comment on the impact of branch instructions in pipelined architecture.
d) What is virtual memory? How virtual address is mapped into real address?

(6+4+4+4)

5.

a) What are the different addressing modes of a general-purpose processor? Explain with suitable examples.
b) Explain Timing and Control of Computer Architecture.

c) Represent the number $(+47.5)_{10}$ as a floating point binary number with 24 bits, where mantissa has 16 bits and the exponent has 8 bits.

d) A computer has a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register part to specify one of 64 registers and an address part.

i) How man bits are there in the operation code, the register code part and the address part?

ii) Draw the instruction word format and indicate the number of bits in each part.

iii) How many bits are there in the data and address inputs of the memory?

(6+4+3+5)

6.

a) Compare and contrast interrupt-initiated data transfer and data transfer under program control without an interrupt.

b) What do you mean by 'direct memory access (DMA)'? Why does DMA have priority over the CPU when both request a memory transfer?

c) Explain Binary adder circuit.

(6+6+6)

7.

a) Explain and differentiate programmed I/O and memory mapped I/O.

b) Explain Arithmetic Logic and Shift Unit.

c) Explain General Register Organization.

(6+6+6)